

Super-K Electronics Upgrade

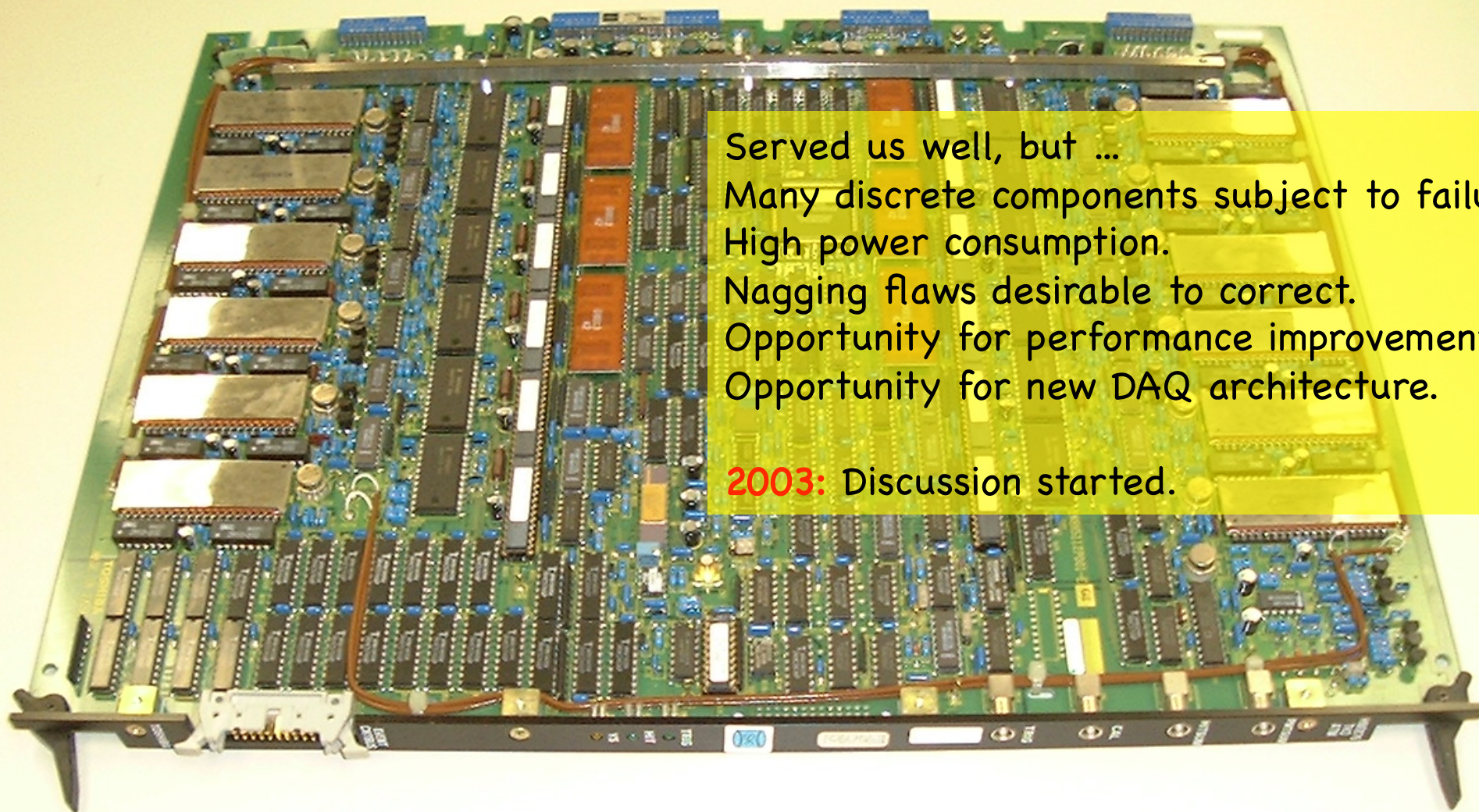
Ed Kearns
Boston U.

LBDUSEL Meeting, UCD, Feb. 28, 2009

About this talk

- I am making no claim regarding electronics for the new detector.
- This is just a report of the most recent effort for a similar detector.
- Rough schedule was:
 - 2004 – Specification, conceptual designs
 - 2005 – R&D and engineering
 - 2006 – Prototyping and testing
 - 2007 – Final tests and production
 - 2008 – Delivery and Installation

Previous Electronics (1996-2007)



Served us well, but ...
Many discrete components subject to failure.
High power consumption.
Nagging flaws desirable to correct.
Opportunity for performance improvement.
Opportunity for new DAQ architecture.

2003: Discussion started.

Plus: Outer Detector instrumented with completely different system: custom front-end plus LeCroy FASTbus TDC.
Unifying design and operation desirable.

Specifications (2004):

- Equal or exceed every spec of previous system:
- High density 12→24 ch/board
- Less deadtime 1 μs →0.4 μs (good for muon decay e)
- Better resolution 8→12 bit
- Wider dynamic range 250 p.e.→1000 p.e.
- Lower noise (reduce hit threshold 0.3 p.e. → 0.1 p.e.)
- Lower power consumption 4W→1W
- More highly integrated
- Keep TKO crate for power
- Ethernet readout (→20x peak data rate)

QBEE

QTC-Based Electronics with Ethernet.

comprised of:

QTC: Charge-to-Time Converter
Custom IC (ICRR/Iwatsu)

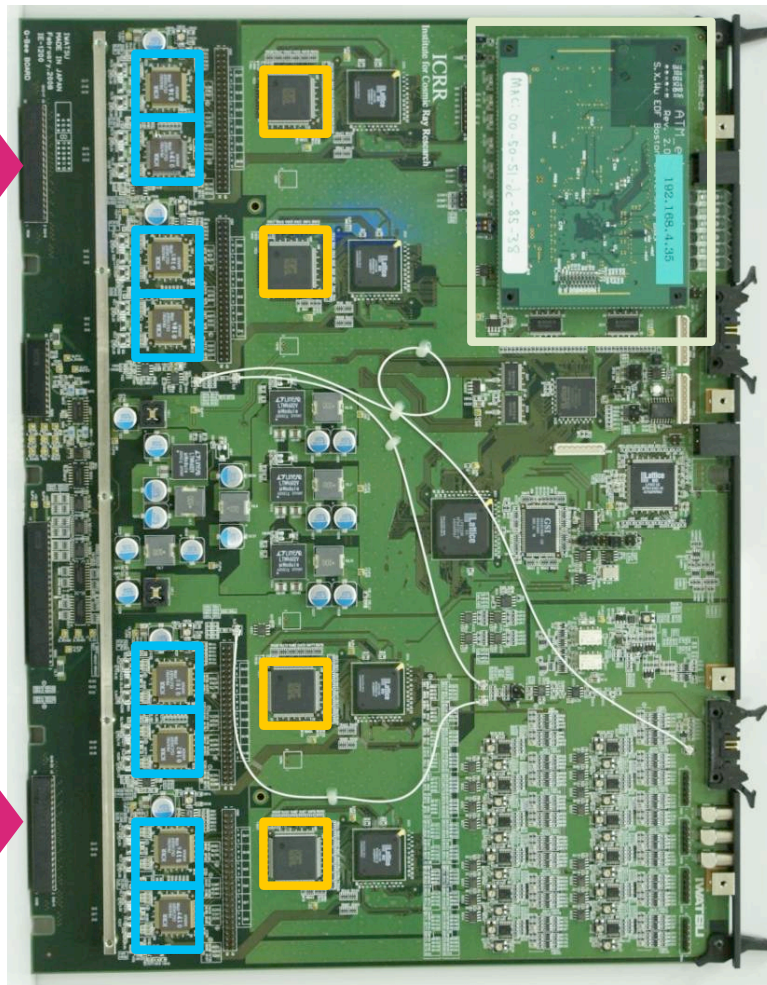
TDC: AMT3 chip (designed for Atlas)

Ethernet Daughtercard
(U.S. group)

SiTCP: Silicon TCP
Firmware implementation of TCP/IP (KEK)

Ethernet Daughtercard

PMT
signal



QTC

TDC

Development

- QTC custom IC and QBEE module designed by Iwatsu Electric Co. in collaboration with scientists from ICRR/U. Tokyo. Development costs seem to be mainly supported by ICRR. QBEE is a quasi-commercial product – eg. RENO is using ~ 50.
- Ethernet daughtercard designed by Boston University. Detailed interface specification exchanged with Iwatsu. Successful collaboration.
- Our (U.S. SK collaborator) marginal cost was \$130/ch.

QBEE(QTC Base Electronics and Ethernet) IE-1200

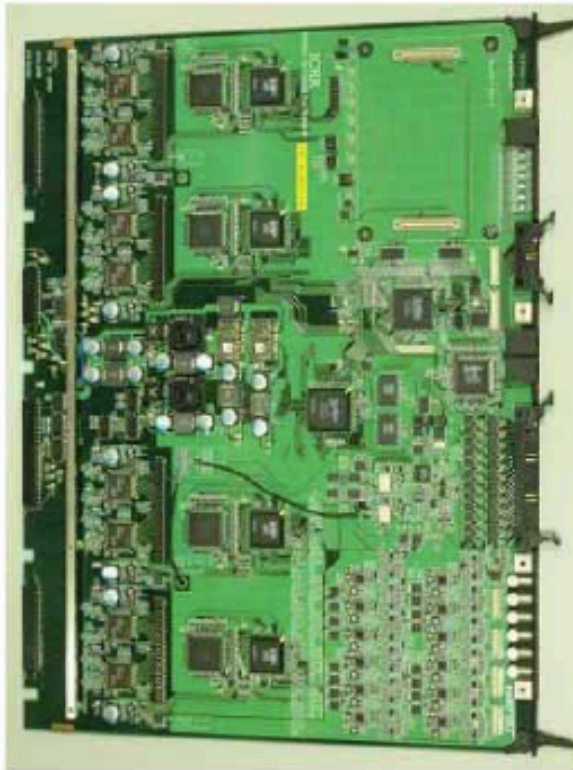


Fig. 1. Photograph of the QBEE. There are 24 input channels. It consists of 8 QTC chips and 4 AMTs.

- A QBEE board is a special board developed as electronics for Super-Kamiokande(SK).
- Eight QTC-LSI and four TDC-LSI are carried, and a QBEE board can process the signal from PMT of total 24ch.
- Each ch has a dynamic range from 0.2PCs to 2500pC(s) with three stages (Large, Medium, and Small).
- It is controllable by Ether-Net by adding Daughter-Board developed at the Boston University. When not using a Daughter board, it can control by the TKO bus.

QTC (Charge-to-Time Converter)

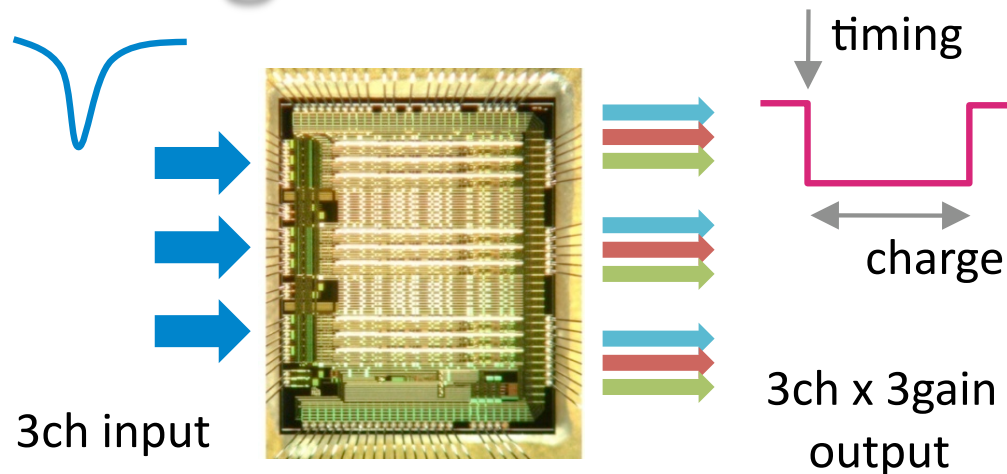


TABLE I
SPECIFICATION OF THE QTC

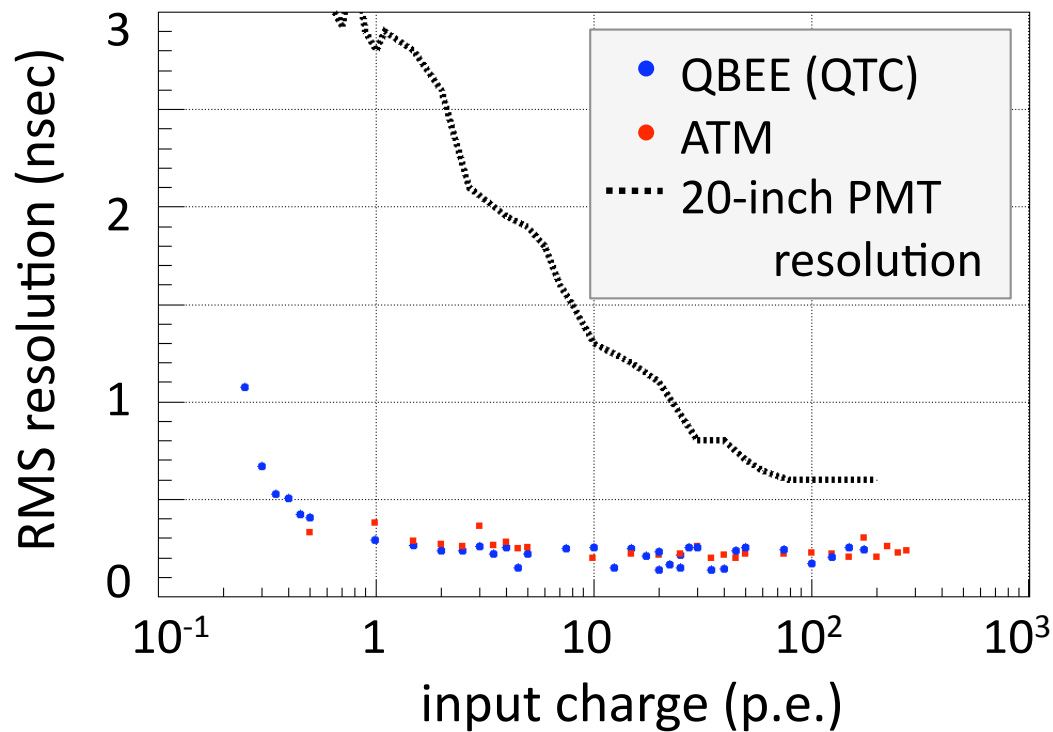
Number of Channels	3
Process Speed	~ 500 ns/hit*
Number of Gain Stages	3
Dynamic Range	0.2 ~ 2500 pC*
Charge Resolution	~ 0.1 pC* (< 50 pC)
Output Level	LVDS
Supply Voltage	+3.3 V
Power Dissipation	< 200 mW/ch
Process	0.35 μ m CMOS
Package	100 pin CQFP

(* : externally adjustable)

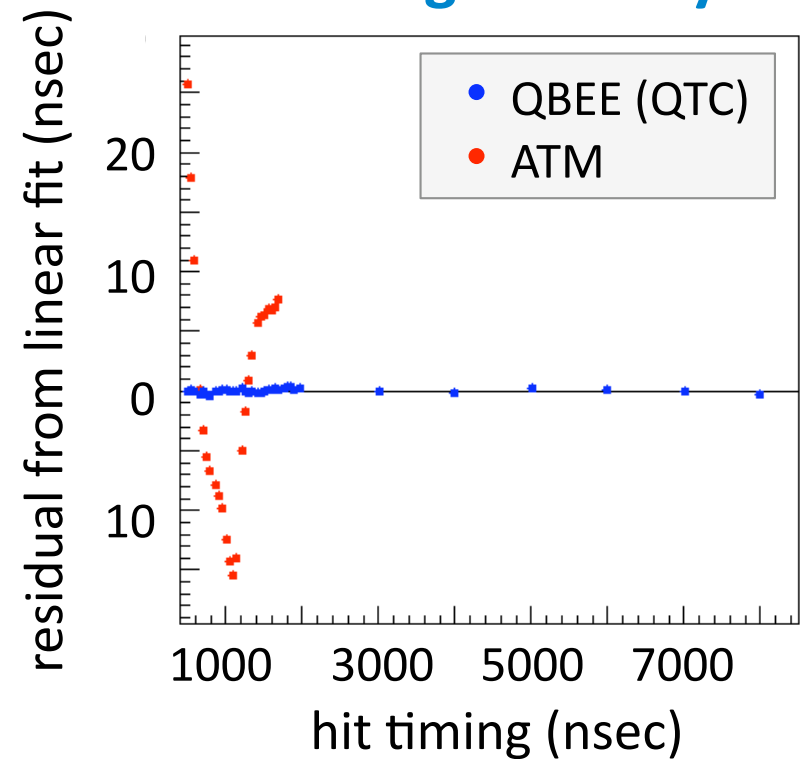
- **Built-in Discriminator**
- **Processing Speed**
 - 400 ns charge integration gate
 - ~1usec hit cycle
- **Dynamic Range**
 - 3 gain stages (1:7:49x)
 - 0.1 ~ 1250 p.e.

QBEE Performance - Timing

Timing Resolution



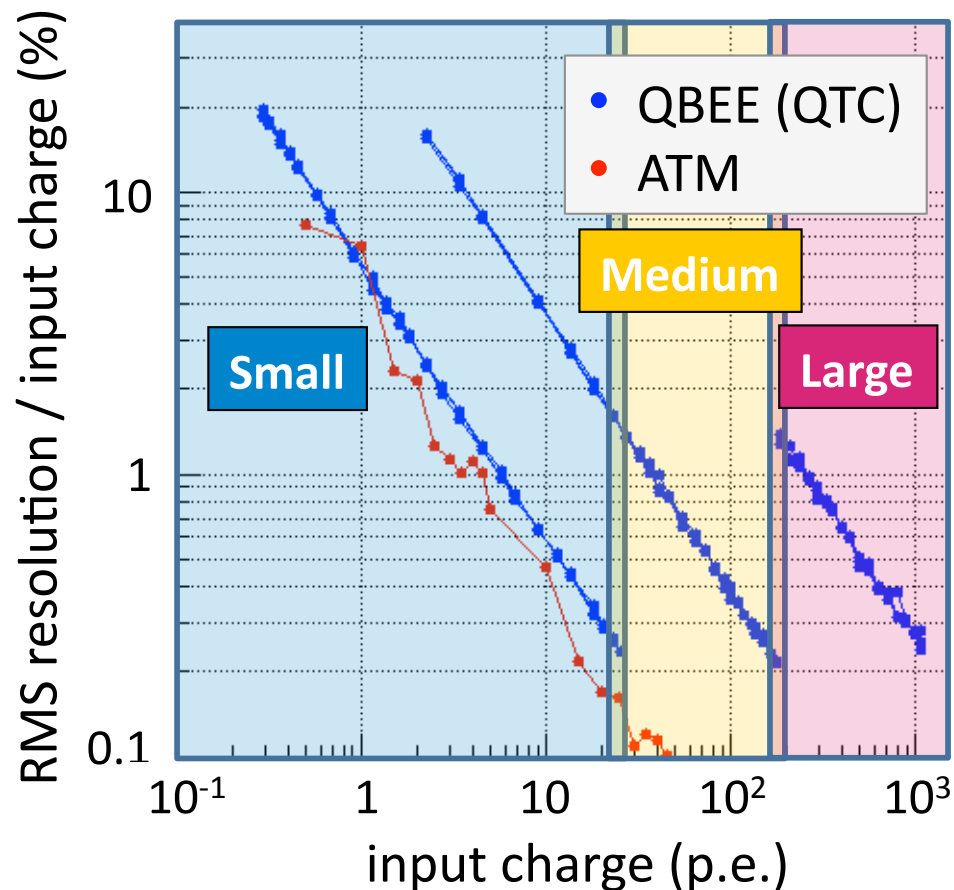
Timing Linearity



0.52 nsec / count

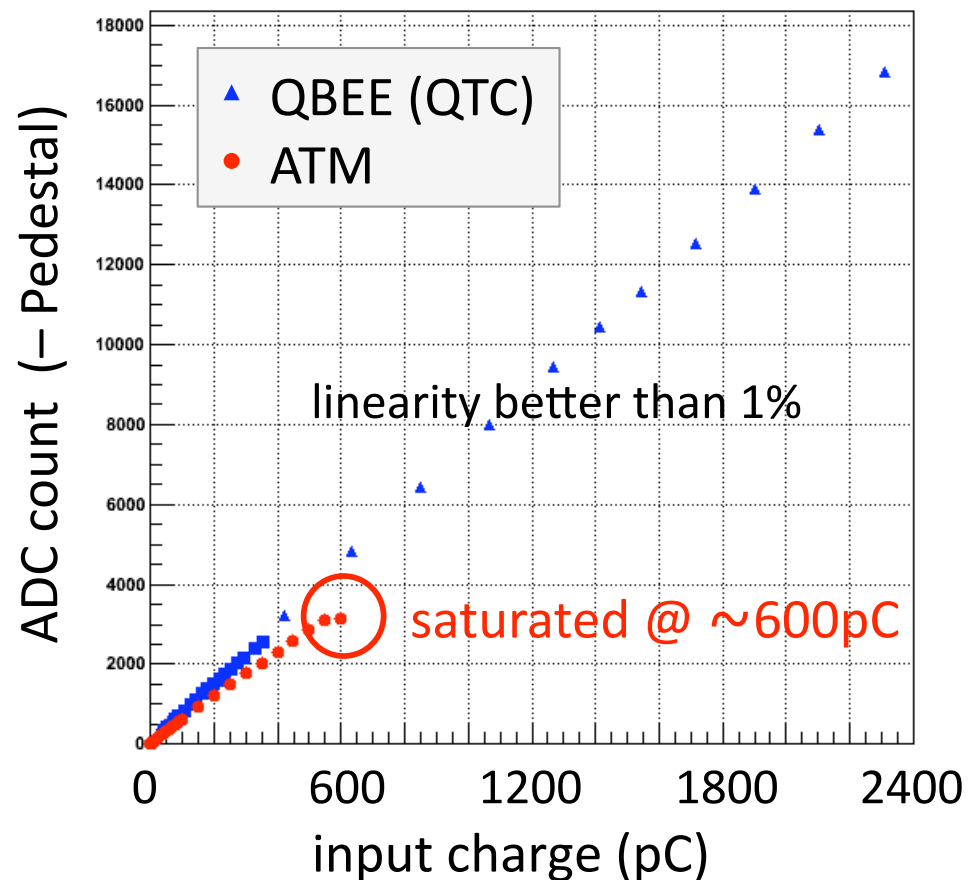
QBEE Performance - Charge

Charge Resolution

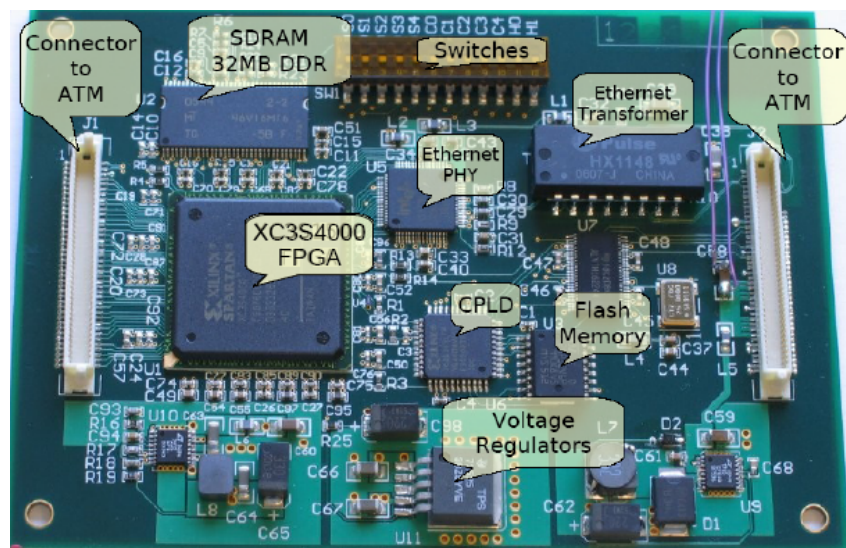


1 p.e. \approx 2 pC

Dynamic Range

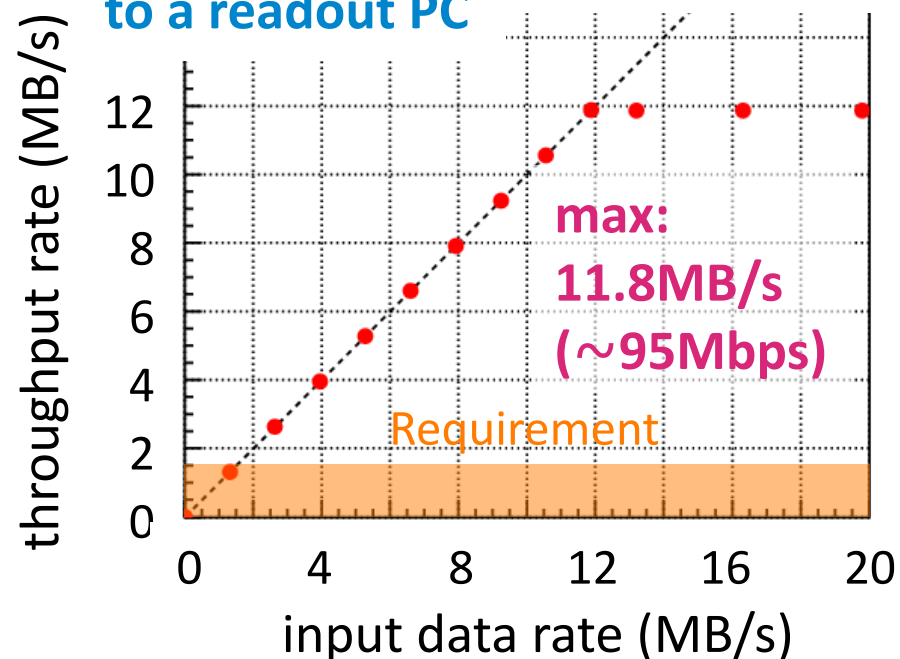


Ethernet Daughtercard + SiTCP



- 100-base T
- 32MB SDRAM
- Set IP by switches
- High speed data readout : TCP
Control : UDP
- Keeps data transfer OFF backplane (noisy)
- Flexible DAQ architecture using commodity network switches
- Can plug into your laptop for testing!

QBEE throughput from analog input to a readout PC



Required data transfer speed :
(PMT dark noise) $10\text{kHz} \times 6\text{byte} \times 24\text{ch}$
 $= 1.5\text{MB/sec/board}$

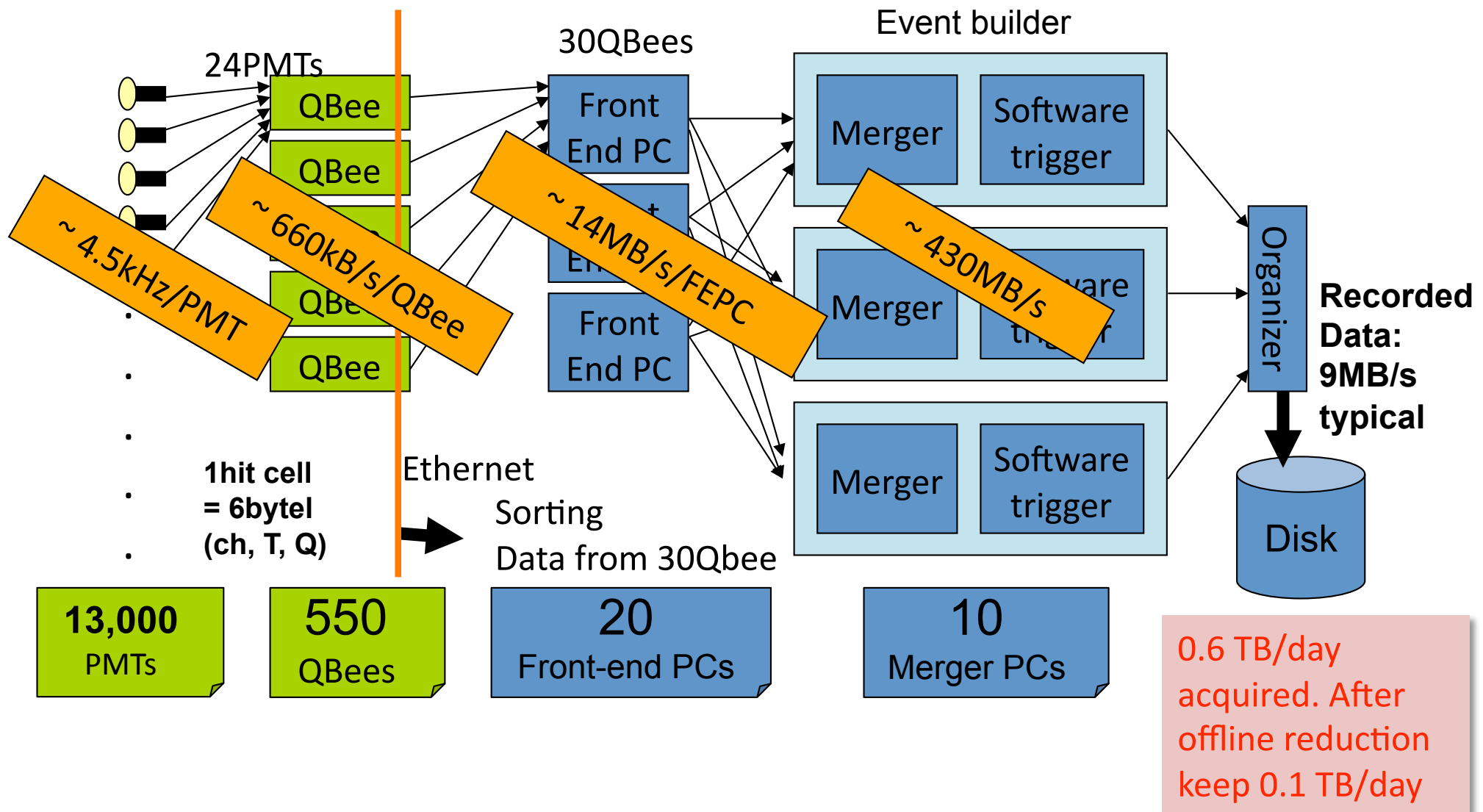
Installed – 9/2008

LAN cables
for readout
and control



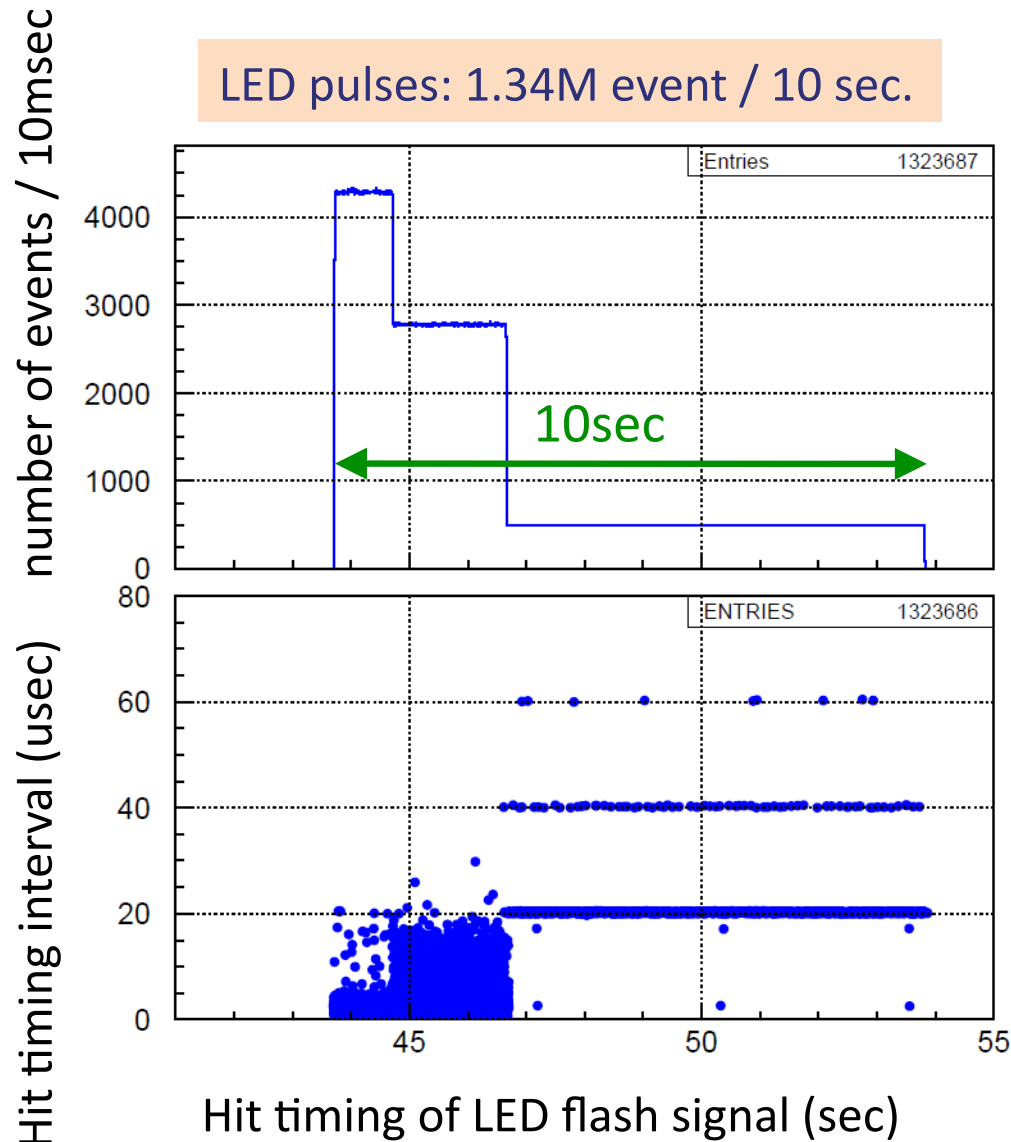
PMT cables come into the back of the TKO crates

Throughput



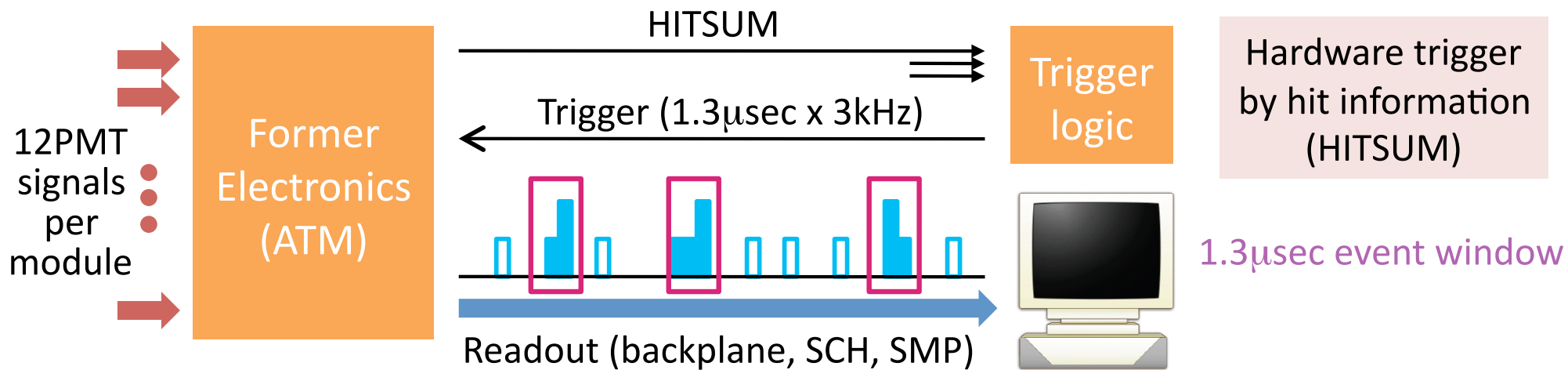
Supernova Burst Test

LED pulses: 1.34M event / 10 sec.

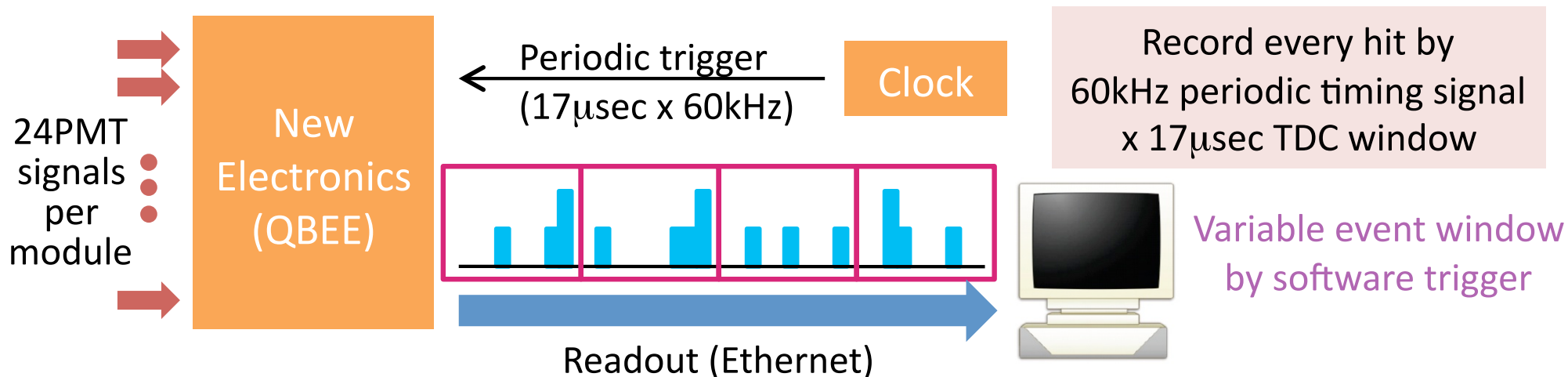


- Electronics and online DAQ ran without stopping.
- No significant dead-time even for 1M event / 10 sec burst
 - > 150 x SN in G.C.
 - > 20 x current system

Old → New: Hardware Trigger → Record Every Hit



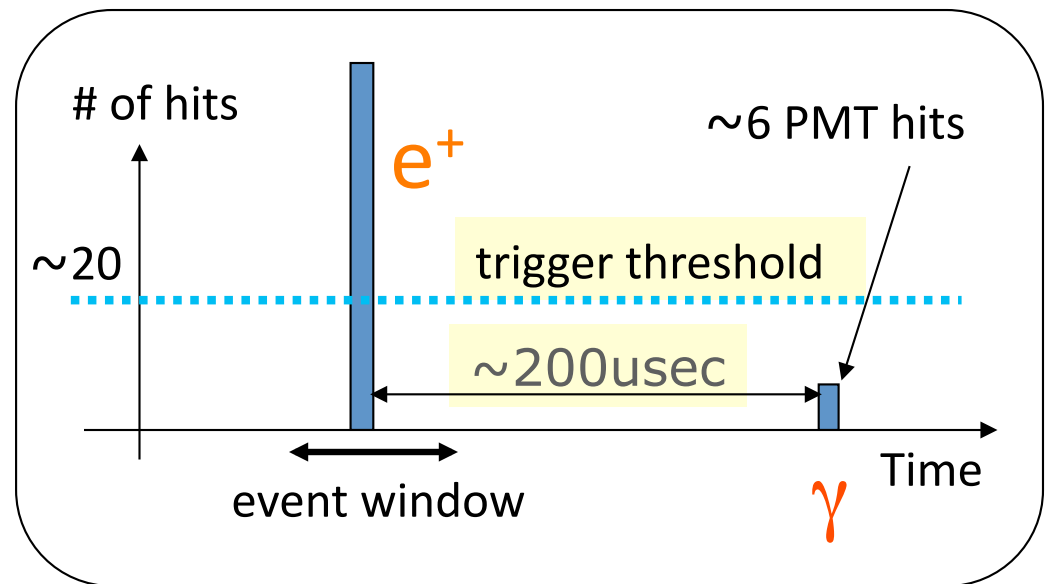
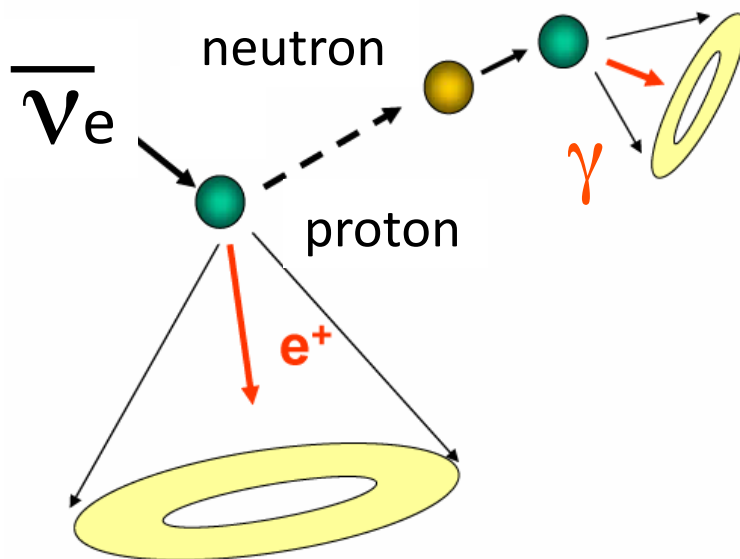
No hardware trigger. Instead record all hits and apply software triggers.



Motivation for Record-Every-Hit

Record low energy events, below hardware trigger threshold

- Diffuse Supernova Neutrino Background



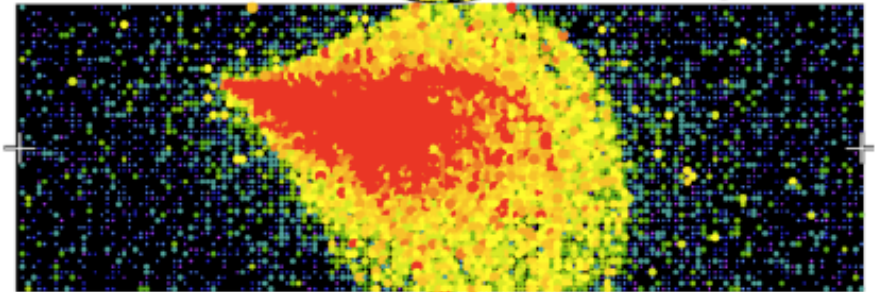
Summary

SK electronics replaced and
DAQ rewritten. Concept to
installation 2004-2008.
In time for T2K.

Super-Kamiokande IV

Run 61671 Sub 3 Ev 382253
38-10-15:15:27:42
inner: 7456 hits, 80531 pc
outer: 248 hits, 1017 pc (in-time)
Trigger ID: 0x1800000f
D wall: 1690.3 cm
Fully-Contained Mode

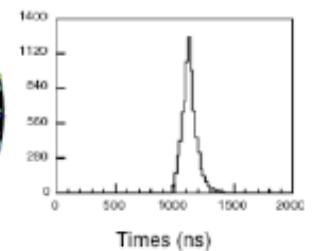
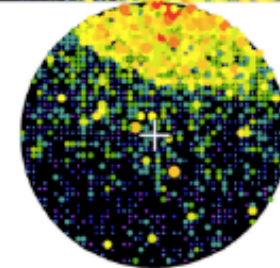
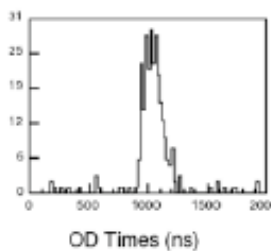
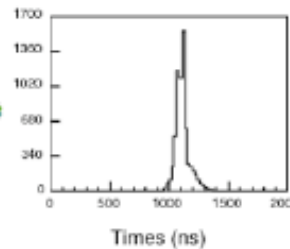
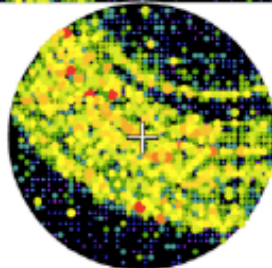
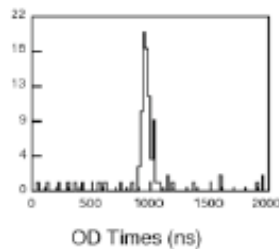
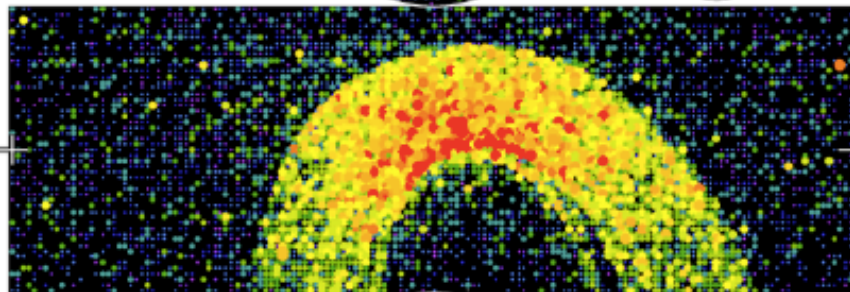
Charge (pe)



Super-Kamiokande IV

Run 61671 Sub 2 Ev 221111
38-10-15:15:28:40
inner: 7450 hits, 42415 pc
outer: 83 hits, 423 pc (in-time)
Trigger ID: 0x1800000f
D wall: 1690.3 cm
Fully-Contained Mode

Charge (pe)



- Operational experience is good so far. We will review the first sizeable data set at the June 2009 collaboration meeting.